

Patch-Clamp Microchip Testing Circuit Interface Design Document

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sdmay18-10

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1 Introduction

1.1 Acknowledgement

This design document was supported by our advisor Dr. Que Long and graduated student Silu Feng. We thank them for their great assistance in this project, although they may not agree with all of the interpretations of this design document.

1.2 Problem and Project Statement

Patch-clamp is a technology in biological engineering field which means to catch cell with tiny clamp and observe the bioelectricity behavior of the cell. Our project is focusing on how to build up a set of electric environment and circuit to provide operational interface between the patch-clamp and electron microscope. With patch-clamp, human will observe a clearer picture about cells, which for our project are neurons, the nerve system cells. This could be done with getting a clear electric current square graph of the currents that generated when ions try to enter and leave the membrane of neurons, and this is what we do for our project to build the interface to capture the current graph. These behaviors of neurons will lead biological engineers to look for many possible cures of some serious nerve diseases that could not be cured right now.

We use PC-ONE Patch/Whole Cell Clamp to build the interface. This clamp equipment is also the main tool we use to build our interface.

1.3 operational Enviroment

The operational environment of Patch-Clamp Microchip Testing Circuit Interface is biological laboratory with complete safety equipments and professional operators. The operation of Patch-Clamp Microchip Testing Circuit Interface must be done safely under required professional assistance.

1.4 Intended Users and uses

Patch-clamp technique can not only be used in neuroscience but also a huge variety of physiological questions. For this technique is still the laboratory technique, so the user for this technique should be the experimenters, who want to know the ion current on the membrane when we apply different voltage or we use different solution in the bath. The most commonly use for this technique is drug discovery. For our project, we will test the different voltage on the neuronal cells to find the way to increase cell viability and make the neuronal cells can split fast. The method can be used on depression treatment, for we can make their neuronal cell more excited than before.

1.5 Assumptions and Limitations

Assumptions:

- The patch-clamp testing circuit can catch two cells at the same time to decrease the testing times.
- The simulation result will be useful to defeat depression .

- The mode can be used multiple times until we finish the project.

Limitations:

- Two semesters to work on this project
- Do not have too much testing samples (neuronal cells). We may fail many times, so it is hard to get the correct answer.
- Do not have appropriate material to reduce the room noise

1.6 Expected End Product and Deliverables

At the end of this semester, we are supposed to deliver a fully set up patch-clamp circuit, which is operational to catch cells and observe the bioelectricity behavior of the cell. The goal is to build up a set of electric environment and circuit to provide operational and functional interface between the patch-clamp and electron microscope. In addition, before April 2018, we are supposed to measure the ion channel potential of cells and the action potential of cells under external stimulations successfully by using the patch-clamp microchip.

2. Specifications and Analysis

2.1 Proposed Design

For our project, we are trying to set up the patch clamp by the manual and documents of patch clamp. For this setting up, we need to connect the patch clamp, mode of cell and simulation.

After setting up the patch clamp, we need to use patch clamp to catch a neuron cell by applying positive and negative voltage on the two sides of the patch clamp and do test on the cell, which include measure the current through the cell.

2.2 Design Analysis

Up to know, we read the manual and document of patch clamp, tried to set up the patch clamp, and helped the graduate to make the mode of cell. The mode of cell has two holes to catch the neuron cells, so we can catch two cells at one time, which can help us get two measured results at one testing.

3 Testing and Implementation

3.1 Interface Specifications

In our project, we need to use PC-one patch/whole cell clamp.

3.2 Hardware and software

PC-one patch/whole cell clamp is one of the most important part in our project. We need to use patch clamp to catch the neuron cells, and test the current and voltage through the cell.

3.3 Process

For the test, we need to apply a positive voltage power supply at one side and a negative voltage power supply at another side, which can help use catch the cells by patch clamp. We also need to apply a voltage through the cell and test the current through the cell, and show the results on the simulation.

3.4 Results

For now, we are in the process of building up the patch-clamp circuit. We are supposed to finish setting up the circuit at the end of this semester. Everything we have done until now has been theoretical and meant to improve the team members understand and knowledge of the project and the process.

4 Closing Material

4.1 Conclusion

Our project is focusing on how to build up a set of electric environment and circuit to provide operational interface between the patch-clamp and electron microscope. With patch-clamp microchip, people could observe a clearer picture about cells, which for our project are neurons, the nerve system cells. This could be done with getting a clear electric current square graph of the currents that generated when ions try to enter and leave the membrane of neurons. We are going to measure the ion channel potential of cells and the action potential of cells under external stimulations after we setting up the patch-clamp microchip successfully. Meanwhile, during the process of experimental measurements, we should figure out a method to store these neuron cells to keep them alive.

4.2 References

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Y Zhao*¹, S Inayat*¹, D A Dikin*², J H Singer*³, R S Ruoff*⁴, and J B Troy*¹, *Patch clamp technique: review of the current state of the art and potential contributions from nanoengineering*, 08 June 2009, DOI: 10.1243/17403499JNN149.

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4.3 Appendices

Any additional information that would be helpful to the evaluation of your design document. If you have any large graphs, tables, or similar that does not directly pertain to the problem but helps support it, include that here. This would also be a good area to include hardware/software manuals used. May include CAD files, circuit schematics, layout etc. PCB testing issues etc. Software bugs etc.